CLAIMS

1. An architected register file system at least configured to utilize a plurality of threads, comprising:

a plurality of register files, wherein each register file of the plurality of register files at least corresponds to at least one thread of the plurality of threads;

a plurality of Status and Control Registers (SCR), wherein each SCR corresponds to at least one register file of the plurality of register files; and

a plurality of control bit sets, wherein each control bit set corresponds to at least one SCR, and wherein each control bit set is at least configured to allow a thread associated with an associated SCR to utilize other register files associated with other threads.

2. The architected register file system of Claim 1, wherein the architected register file system further comprises a decoder, wherein the decoder at least determines desired operations for an instruction.

3. The architected register file system of Claim 1, wherein plurality of control bits further comprise a plurality of bit doublets, wherein a first bit of a bit doublet corresponds to a read function, and wherein a second bit of the bit doublet corresponds to a write function.

4. The architected register file system of Claim 3, wherein the architected register file system further comprises:

an address control, wherein the address control at least determines addresses with the plurality of register files; and

at least one execution unit, wherein the execution is at least configured to perform the operations of a input instruction within the plurality of register files.

5. The architected register file system of Claim 3, wherein the plurality of bit doublets further comprises that each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread.

6. The architected register file system of Claim 5, wherein each bit doublet of the plurality of bit doublets further comprises:

at least one bit is at least configured to correspond to a read function, wherein a logic high or '1' enables the first thread to read from another register file; and

at least one bit is at least configure to correspond to a write function, wherein a logic high or '1' enables the first thread to write to another register.

7. A method for utilizing a plurality of register files with associated SCRs in a multithread system, wherein each register file is at least associated with one thread of a plurality of threads, comprising:

receiving an instruction for a first thread of the plurality of threads, wherein the first thread is at least associated with a first SCR;

decoding the instruction to at least determine performance operations;

determining if the first thread is enabled to at least utilize register files associated with other threads; and

executing the instruction, wherein the step of executing at least utilizes whatever register files that are enabled.

8. The method of Claim 7, wherein the step of determining if the first thread is enabled, further comprises measuring logical levels of control bits associated with the first SCR, wherein the control bits comprise a plurality of bit doublets, and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread.

9. The method of Claim 8, wherein the step of measuring further comprises determining if any bits are '1'

or logic high, wherein the '1' or the logic high enables the first thread to read or write to another register file.

10. A computer program product for utilizing a plurality of register files with associated SCRs in a multithread system, wherein each register file is at least associated with one thread of a plurality of threads, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for receiving an instruction for a first thread of the plurality of threads, wherein the first thread is at least associated with a first SCR;

computer code for decoding the instruction to at least determine performance operations;

computer code for determining if the first thread is enabled to at least utilize register files associated with other threads; and

computer code for executing the instruction, wherein the step of executing at least utilizes whatever register files that are enabled.

11. The computer program product of Claim 10, wherein the computer code for determining if the first thread is enabled, further comprises computer code for measuring logical levels of control bits associated with the first

SCR, wherein the control bits comprise a plurality of bit doublets, and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread.

12. The computer program product of Claim 11, wherein the computer code for measuring further comprises determining if any bits are '1' or logic high, wherein the '1' or the logic high enables the first thread to read or write to another register file.

13. A processor for utilizing a plurality of register files with associated SCRs in a multithread system, wherein each register file is at least associated with one thread of a plurality of threads, the processor including a computer program comprising:

computer code for receiving an instruction for a first thread of the plurality of threads, wherein the first thread is at least associated with a first SCR;

computer code for decoding the instruction to at least determine performance operations;

computer code for determining if the first thread is enabled to at least utilize register files associated with other threads; and

computer code for executing the instruction, wherein the step of executing at least utilizes whatever register files that are enabled.

14. The computer code of Claim 13, wherein the computer code for determining if the first thread is enabled, further comprises computer code for measuring logical levels of control bits associated with the first SCR, wherein the control bits comprise a plurality of bit doublets, and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread.

15. The computer code of Claim 14, wherein the computer code for measuring further comprises determining if any bits are '1' or logic high, wherein the '1' or the logic high enables the first thread to read or write to another register file.